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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/039,794	10/19/2001	Heui Gi Son	2080-3-44	9216

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LEE, HONG, DEGERMAN, KANG & SCHMADEKA, P.C.
801 SOUTH FIQUEROA STREET
14TH FLOOR
LOS ANGELES, CA 90017

EXAMINER	
ODOM, CURTIS B	

ART UNIT	PAPER NUMBER
2634	

DATE MAILED: 11/29/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/039,794	SON ET AL.	
	Examiner	Art Unit	
	Curtis B. Odom	2634	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 September 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 October 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claim 11-14 are objected to because of the following informalities: "RDS" and "RLL" and suggested to be defined in claim 11. Appropriate correction is required.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1, 4-8, 10, 11, 14, and 18-20 are rejected under 35 U.S.C. 102(b) as being anticipated by Tanaka et al. (U. S. Patent No. 5, 912, 869).

Regarding claim 1, Tanaka et al. discloses a method of converting digital data, comprising the steps of:

binding (column 12, lines 18-64) input digital data into unit blocks comprising a plurality of bytes;

modulation-coding (column 12, line 65-column 13, line 30) each byte of the unit blocks according a code conversion table; and

allocating (column 13, lines 9-17, see also U. S. Patent No. 4, 728, 929, incorporated by reference) at least one merging bit in a block unit for the modulation-coded unit block.

Regarding claim 4, which inherits the limitations of claim 1, Tanaka et al. discloses each of the modulation-coded input data block is encoded into a code word of a fifteen bit length by an 8/15 conversion table (column 13, lines 11-30).

Regarding claim 5, which inherits the limitations of claim 1, Tanaka et al. discloses a RDS (column 17, line 50-column 18, line 21, DSV) of a present input data block (frame 2) is compared to a RDS of a previous unit block (frame 1) to allocate the merging bit (code sequence for suppressing DC component bias, see column 13, lines 11-17) so that the RDS is minimized (column 18, lines 3-21) without violating RLL restraints (column 6, lines 41-51).

Regarding claim 6, which inherits the limitations of claim 5, Tanaka et al. discloses the at least one merging bit is primarily outputted (column 13, lines 11-17), and modulation-coded present input data block is outputted (Fig. 8, block 806), and simultaneously the RDS up to the current unit block is simultaneously updated to prepare for allocation of at least one merging bit for a next unit block (column 22, lines 3-25).

Regarding claim 7, Tanaka et al. discloses a method of digital data conversion, comprising the steps of:

performing (column 12, line 65-column 13, line 30) 8/15 modulation-coding to an input data block in the unit of m byte and simultaneously producing a RDS of the input data block (Fig. 8, block 807, column 17, line 50-column 18, line 21 and column 21, line 54-column 22, line 25));

evaluating (column 17, line 50-column 18, line 21) the RDS of the input data block (frame 2) and an RDS of the previous block (frame 1) to select a merging bit (code sequence to suppress dc bias, see column 13, lines 11-17); and

outputting (column 13, lines 1-17) the selected at least one merging bit, following by modulation-coded input data block (column 18, lines 3-21, type information 1 or 2 and the beginning of the frame), and updating the RDS for selecting at least one merging bit for a next input data block (column 22, lines 3-25).

Regarding claim 8, Tanaka et al. discloses binding (column 12, lines 18-64) input digital data into unit blocks comprising a plurality of bytes and modulation-coding each of the unit blocks (column 12, line 65-line 30);

allocating (column 13, lines 9-17, see also U. S. Patent No. 4, 728, 929, incorporated by reference) at least one merging bit in a block unit for the modulation-coded unit block;

recording (column 12, lines 24-56, column 14, lines 10-40, and column 26, lines 11-16 a byte-unit information indicating the number of the bytes comprising each of the unit blocks together with data added with the at least one merging bit after modulation-coding, wherein the synchronization code includes byte-unit information (column 26, lines 11-16); and

performing (column 26, lines 11-16) decoding for the corresponding block by using the recorded byte-unit information.

Regarding claims 10, 11, 14, 18-20 the claimed subject matter includes features corresponding to subject matter mentioned in the above rejection of claims 1 and 4-6 which is applicable hereto.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 2 ,9, 12 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tanaka et al. (U. S. Patent No. 5, 912, 869).

Regarding claims 2, 9, 12, and 15, Tanaka et al. does not discloses each unit (frame) comprises of three to seven bits. However, it would have been obvious to one skilled in the art at the time the invention was made that a unit (frame) length depends on the amount of data which needs to be recorded or the recording medium. Therefore, it would have also been obvious that these specification can vary from recording to recording. Thus, the number of bytes in a frame does not constitute patentability.

6. Claims 3, 13, 16 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tanaka et al. (U. S. Patent No. 5, 912, 869) in view of Immink (U. S. 5, 920, 272).

Regarding claims 3, 13, 16 and 17 Tanaka et al. discloses allocating one merging bit for each codeword (column 13, lines 9-17), but does not disclose three merging bits are allocated.

Immink discloses allocating three merging bits for each codeword such that even regions of transitions between two code words satisfy the run length constraint (dk) and maintain a constant running digital sum. Therefore, it would have been obvious to one skilled in the art at the time the invention was made to modify the method as taught by Tanaka et al. with the teachings of Immink and allocate three merging bits to maintain a constant digital sum in order to further help remove any non-desired low frequency and DC components (column 1, lines 17-53).

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Shimpuku et al. (U. S. Patent No. 5, 781, 131) and Ko (U. S. Patent No. 5, 748, 119) disclose allocation merging bits to a codeword to control a DC bias and minimize the RDS.

Okazaki et al. (U. S. Patent No. 5, 870, 037) discloses allocation three merging bits for each codeword.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Curtis B. Odom whose telephone number is 571-272-3046. The examiner can normally be reached on Monday- Friday, 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Stephen Chin can be reached on 571-272-3056. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Curtis Odom
November 22, 2005

STEPHEN CHIN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600